WHAT IS CLAIMED IS:

1. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISTFTs (Metal Insulator Semiconductor Thin Film Transistors) having semiconductor layers comprised of polysilicon,

said level converter circuit comprising:

a pair of a first NMISTFT (N-channel type Metal Insulator Semiconductor Thin Film Transistor) and a first PMISTFT (P-channel type Metal Insulator Semiconductor Thin Film Transistor),

each of said first NMISTFT and said first PMISTFT having both a gate terminal thereof and a first terminal thereof coupled to an input terminal for receiving an input pulse via a first capacitance;

a pair of a second NMISTFT and a second PMISTFT,

each of said second NMISTFT and said second PMISTFT having a second terminal thereof coupled to said input terminal via a second capacitance;

a third PMISTFT having a gate terminal thereof coupled to said gate terminals and said first terminals of said first NMISTFT and said first PMISTFT;

a third NMISTFT having a gate terminal thereof coupled to said second terminals of said second NMISTFT and said second PMISTFT,

a first terminal of said third PMISTFT, a second terminal of said first NMISTFT, and a second terminal of said first PMISTFT being coupled to a high-voltage power supply line,

a second terminal of said third NMISTFT, a gate terminal and a first terminal of said second NMISTFT, a gate terminal and a first terminal of said second PMISTFT being coupled to a low-voltage power supply line, and

a first junction point between a second terminal of said third PMISTFT and a first terminal of said third NMISTFT being connected to an output terminal of said level converter circuit.

2. A display device according to claim 1, further comprising a series combination of a fourth PMISTFT and a fourth NMISTFT, wherein

a first terminal of said fourth PMISTFT is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT are coupled to said first junction point, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT being connected to said output terminals of said level converter circuit.

3. A display device according to claim 1, further comprising a plurality of series combinations of a fourth PMISTFT and a fourth NMISTFT,

wherein said plurality of series combination are cascaded in a plurality of stages,

a first terminal of said fourth PMISTFT of each of said plurality of series combinations is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT of each of said plurality of series combinations is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in a first one of said plurality of stages counting from said first junction point are coupled to said first junction point,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in said plurality of stages excluding said first stage are coupled to junction points between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT of immediately preceding ones of said plurality of stages, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT in a final one of said plurality of stages being connected to said output terminal of said level converter circuit.

4. A display device according to claim 1, wherein at least one of said first NMISTFT, said first PMISTFT, said second NMISTFT and said second PMISTFT is substituted by one of a diode and a series combination of a diode and a resistor.

5. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISTFTs (Metal Insulator Semiconductor Thin Film Transistors) having semiconductor layers comprised of polysilicon, said level converter circuit having a plurality of stages arranged in series,

each of said plurality of stages comprising:

a pair of a first NMISTFT (N-channel type Metal Insulator Semiconductor Thin Film Transistor) and a first PMISTFT (P-channel type Metal Insulator Semiconductor Thin Film Transistor),

each of said first NMISTFT and said first PMISTFT having both a gate terminal thereof and a first terminal thereof coupled to an input terminal for receiving an input pulse via a first capacitance;

a pair of a second NMISTFT and a second PMISTFT,

each of said second NMISTFT and said second PMISTFT having a second terminal thereof coupled to said input terminal via a second capacitance;

a third PMISTFT having a gate terminal thereof coupled to said gate terminals and said first terminals of said first NMISTFT and said first PMISTFT;

a third NMISTFT having a gate terminal thereof coupled to said second terminals of said second NMISTFT and said second PMISTFT,

a first terminal of said third PMISTFT, a second terminal of said first NMISTFT, and a second terminal of said first PMISTFT being coupled to a high-voltage power supply line,

a second terminal of said third NMISTFT, a gate terminal and a first terminal of said second NMISTFT, a gate terminal and a first terminal of said second PMISTFT being coupled to a low-voltage power supply line, and

a first junction point between a second terminal of said third PMISTFT and a first terminal of said third NMISTFT being connected to an output terminal.

6. A display device according to claim 5, further comprising at least one stage of a circuit including a fourth PMISTFT and a fourth NMISTFT,

wherein said at least one stage of said circuit is coupled between successive ones of said plurality of stages,

gate terminals of said fourth PMISTFT and said fourth NMISTFT are connected to an input terminal of said circuit,

one terminal of said fourth PMISTFT and one terminal of said fourth NMISTFT are connected to an input terminal of said circuit,

another terminal of said fourth PMISTFT is coupled to said high-voltage power supply line, and

another terminal of said fourth NMISTFT is coupled to said low-voltage power supply line.

7. A display device according to claim 6, further comprising at least one stage of a circuit including a fifth PMISTFT and a fifth NMISTFT,

wherein said at least one stage of said circuit is coupled to a final one of said plurality of stages,

gate terminals of said fifth PMISTFT and said fifth NMISTFT are connected to an input terminal of said circuit,

one terminal of said fifth PMISTFT and one terminal of said fifth NMISTFT are connected to an output terminal of said circuit,

another terminal of said fifth PMISTFT is coupled to said high-voltage power supply line, and

another terminal of said fifth NMISTFT is coupled to said low-voltage power supply line.

8. A display device according to claim 5, further comprising at least one stage of a circuit including a fourth PMISTFT and a fourth NMISTFT,

wherein said at least one stage of said circuit is coupled to a final one of said plurality of stages,

gate terminals of said fourth PMISTFT and said fourth NMISTFT are connected to an input terminal of said circuit,

one terminal of said fourth PMISTFT and one terminal of said fourth NMISTFT are connected to an output terminal of said circuit,

another terminal of said fourth PMISTFT is coupled to said high-voltage power supply line, and

another terminal of said fourth NMISTFT is coupled to said low-voltage power supply line.

9. A display device according to claim 5, wherein at least one of said first NMISTFT, said first PMISTFT, said second NMISTFT and said second PMISTFT is substituted by one of a diode and a series combination of a diode and a resistor.

10. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISTFTs (Metal Insulator

Semiconductor Thin Film Transistors) of a same conductivity type and having semiconductor layers comprised of polysilicon,

said level converter circuit comprising a first MISTFT, a second MISTFT, and a third MISTFT,

first terminals of said first MISTFT and said second MISTFT being coupled to an input terminal for receiving an input pulse,

gate terminals of said first MISTFT and said second MISTFT being coupled to a fixed-voltage power supply line,

a second terminal of said first MISTFT being coupled to a gate terminal of said third MISTFT and a first terminal of a capacitor,

a second terminal of said third MISTFT being coupled to a high-voltage power supply line,

a first terminal of said third MISTFT being coupled to a second terminal of said second MISTFT, and

a junction point of said second terminal of said second MISTFT, said first terminal of said third MISTFT, and a second terminal of said capacitor being connected to an output terminal of said level converter circuit.

11. A display device according to claim 10, wherein said gate terminal of said first MISTFT is coupled to said fixed-voltage power supply line via a resistor, and is also coupled to said input terminal via a capacitor.

12. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit

formed on an insulating substrate and comprised of MISTFTs (Metal Insulator Semiconductor Thin Film Transistors) of a same conductivity type and having semiconductor layers comprised of polysilicon,

said level converter circuit comprising a first MISTFT, a second MISTFT, and a third MISTFT,

first terminals of said first MISTFT and said second MISTFT being coupled to an input terminal for receiving an input pulse,

a gate terminal of said first MISTFT being coupled to a fixed-voltage power supply line,

a gate terminal of said second MISTFT being supplied with a pulse equal in magnitude and opposite in phase with respect to said input pulse,

a second terminal of said first MISTFT being coupled to a gate terminal of said third MISTFT and a first terminal of a capacitor,

a first terminal of said third MISTFT being coupled to a high-voltage power supply line, and

a junction point of a second terminal of said second MISTFT, a second terminal of said third MISTFT, and a second terminal of said capacitor being connected to an output terminal of said level converter circuit.

13. A display device according to claim 12, wherein said gate terminal of said first MISTFT is coupled to said fixed-voltage power supply line via a resistor, and is also coupled to said input terminal via a capacitor.

14. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISTFTs (Metal Insulator Semiconductor Thin Film Transistors) of a same conductivity type and having semiconductor layers comprised of polysilicon,

said level converter circuit having a plurality of stages arranged in series,

each of said plurality of stages comprising:

a first MISTFT, a second MISTFT, and a third MISTFT,

first terminals of said first MISTFT and said second MISTFT being coupled to an input terminal for receiving an input pulse,

a gate terminal of said first MISTFT being coupled to a fixed-voltage power supply line,

a gate terminal of said second MISTFT being supplied with a pulse equal in magnitude and opposite in phase with respect to said input pulse,

a second terminal of said first MISTFT being coupled to a gate terminal of said third MISTFT and a first terminal of a capacitor,

a first terminal of said third MISTFT being coupled to a high-voltage power supply line, and

a junction point of a second terminal of said second MISTFT, a second terminal of said third MISTFT, and a second terminal of said capacitor being connected to an output terminal.

15. A display device according to claim 14, wherein said gate terminal of said first MISTFT in at least one of said plurality of stage is coupled to said high-voltage power supply line.

16. A display device according to claim 15, wherein said gate terminal and said second terminal of said second MISTFT in at least one of said plurality of stages is coupled together via a capacitor.

17. A display device according to claim 14, wherein said gate terminal and said second terminal of said second MISTFT in at least one of said plurality of stages is coupled together via a capacitor.

18. A display device according to claim 14, wherein said gate terminal of said first MISTFT in a first stage in order of said plurality of stages is coupled to said input terminal of said first stage.

19. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISTFTs (Metal Insulator Semiconductor Thin Film Transistors) having semiconductor layers comprised of polysilicon,

said level converter circuit comprising:

a pair of a first NMISTFT (N-channel type Metal Insulator Semiconductor Thin Film Transistor) and a first PMISTFT (P-channel type Metal Insulator Semiconductor Thin Film Transistor),

each of said first NMISTFT and said first PMISTFT having both a gate terminal thereof and a first terminal thereof coupled to an input terminal for receiving an input pulse via a first capacitance;

a pair of second NMISTFT and a second PMISTFT, each of said second NMISTFT and said second PMISTFT having a second terminal thereof and a gate terminal thereof coupled to said input terminal via a second capacitance;

a third PMISTFT having a gate terminal thereof coupled to said gate terminals and said first terminals of said first NMISTFT and said first PMISTFT;

a third NMISTFT having a gate terminal thereof coupled to said second terminals and said gate terminals of said second NMISTFT and a said second PMISTFT,

a first terminal of said third PMISTFT, a second terminal of said first NMISTFT, and a second terminal of said first PMISTFT being coupled to a high-voltage power supply line,

a second terminal of said third NMISTFT, a first terminals of said second NMISTFT, and a first terminal of said second PMISTFT being coupled to a low-voltage power supply line, and

a first junction point between a second terminal of said third PMISTFT and a first terminal of said third NMISTFT being connected to an output terminal of said level converter circuit.

20. A display according to claim 19, further comprising a series combination of a fourth PMISTFT and a fourth NMISTFT, wherein

a first terminal of said fourth PMISTFT is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT are coupled to said first junction point, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT being connected to said output terminal of said level converter circuit.

21. A display device according to claim 19, further comprising a plurality of series combinations of a fourth PMISTFT and a fourth NMISTFT,

wherein said plurality of series combination are cascaded in a plurality of stages,

a first terminal of said fourth PMISTFT of each of said plurality of series combinations is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT of each of said plurality of series combinations is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in a first one of said plurality of stages counting from said first junction point are coupled to said first junction point,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in said plurality of stages excluding said first stage are coupled to junction point between a second terminal of said fourth PMISTFT and said first terminal of said fourth NMISTFT of immediately preceding ones of said plurality of stages, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT in a final one of said plurality of stages being connected to said output terminal of said level converter circuit.

22. A display device according to claim 19, wherein at least one of said first NMISTFT, said first PMISTFT, said second NMISTFT and said second PMISTFT is substituted by one of a diode and a series combination of a diode and a resistor.

23. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISFITS (Metal Insulator Semiconductor Thin Film Transistors) having semiconductor layers comprised of polysilicon,

said level converter circuit comprising:

a pair of a first NMISTFT (N-channel type Metal Insulator Semiconductor Thin Film Transistor) and a first PMISTFT (P-channel type Metal Insulator Semiconductor Thin Film Transistor),

each of said first NMISTFT and said first PMISTFT having both a gate terminal thereof and a first terminal thereof coupled to an input terminal for receiving an input pulse via a first capacitance;

a pair of a second NMISTFT and a second PMISTFT,

each of said second NMISTFT and said second PMISTFT having a second terminal thereof coupled to said input terminal via a second capacitance;

a third PMISTFT having a gate terminal thereof coupled to said first terminals of said first NMISTFT and said first PMISTFT;

a third NMISTFT having a gate terminal thereof coupled to said second terminals of said second NMISTFT and said second PMISTFT,

a first terminal of said third PMISTFT, a gate terminal and a second terminal of said first NMISTFT, and a gate terminal and a second terminal of said first PMISTFT being coupled to a high-voltage power supply line,

a second terminal of said third NMISTFT, a gate terminal and a first terminal of said second NMISTFT, a gate terminal and a first terminal of said second PMISTFT being coupled to a low-voltage power supply line, and

a first junction point between a second terminal of said third PMISTFT and a first terminal of said third NMISTFT being connected to an output terminal of said level converter circuit.

24. A display device according to claim 23, further comprising a series combination of a fourth PMISTFT and a fourth NMISTFT, wherein

a first terminal of said fourth PMISTFT is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT are coupled to said first junction point, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT being connected to said output terminal of said level converter circuit.

25. A display device according to claim 23, further comprising a plurality of series combinations of a fourth PMISTFT and a fourth NMISTFT,

wherein said plurality of series combination are cascaded in a plurality of stages,

a first terminal of said fourth PMISTFT of each of said plurality of series combinations is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT of each of said plurality of series combinations is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in a first one of said plurality of stages counting from said first junction point are coupled to said first junction point,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in said plurality of stages excluding said first stage are coupled to junction points between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT of immediately preceding ones of said plurality of stages, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT in a final one of said plurality of stages being connected to said output terminal of said level converter circuit.

26. A display device according to claim 23, wherein at least one of said first NMISTFT, said first PMISTFT, said second NMISTFT and said second PMISTFT is substituted by one of a diode and a series combination of a diode and a resistor.

27. A display device including a plurality of pixels and a driver circuit to drive said plurality of pixels, said driver circuit including a level converter circuit formed on an insulating substrate and comprised of MISTFTs (Metal Insulator Semiconductor Thin Film Transistors) having semiconductor layers comprised of polysilicon,

said level converter circuit comprising:

a pair of a first NMISTFT(N-channel type Metal Insulator Semiconductor Thin Film Transistor) and a first PMISTFT (P-channel type Metal Insulator Semiconductor Thin Film Transistor),

each of said first NMISTFT and said first PMISTFT having both a gate terminal thereof and a first terminal thereof coupled to an input terminal for receiving an input pulse via a first capacitance;

a pair of a second NMISTFT and a second PMISTFT,

each of said second NMISTFT and a second PMISTFT having a second terminal thereof and a gate terminal thereof coupled to said input terminal via a second capacitance;

a third PMISTFT having a gate terminal thereof coupled to said first terminals of said first NMISTFT and said first PMISTFT;

a third NMISTFT having a gate terminal thereof coupled to said second terminals and said gate terminals of said second NMISTFT and said second PMISTFT,

a first terminal of said third PMISTFT, a gate terminal and a second terminal of said first NMISTFT, and a gate terminal and a second terminal of said first PMISTFT being coupled to a high-voltage power supply line,

a second terminal of said third NMISTFT, a first terminal of said second NMISTFT, and a first terminal of said second PMISTFT being coupled to a low-voltage power supply line, and

a first junction point between a second terminal of said third PMISTFT and a first terminal of said third NMISTFT being connected to an output terminal of said level converter circuit.

28. A display device according to claim 27, further comprising a series combination of a fourth PMISTFT and a fourth NMISTFT, wherein

a first terminal of said fourth PMISTFT is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT are coupled to said first junction point, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT being connected to said output terminal of said level converter circuit.

29. A display device according to claim 27, further comprising a plurality of series combination of a fourth PMISTFT and a fourth NMISTFT,

wherein said plurality of series combination are cascaded in a plurality of stages,

a first terminal of said fourth PMISTFT of each of said plurality of series combination is coupled to said high-voltage power supply line,

a second terminal of said fourth NMISTFT of each of said plurality of series combinations is coupled to said low-voltage power supply line,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in a first one of said plurality of stages counting from said first junction point are coupled to said first junction point,

gate terminals of said fourth PMISTFT and said fourth NMISTFT in said plurality of stages excluding said first stage are coupled to junction points between a second terminal of said fourth PMISTFT and said terminal of said fourth NMISTFT of immediately preceding ones of said plurality of stages, and

a second junction point between a second terminal of said fourth PMISTFT and a first terminal of said fourth NMISTFT in a final one of said plurality of stages being connected to said output terminal of said level converter circuit.

30. A display device according to claim 27, wherein at least one of said first NMISTFT, said first PMISTFT, said second NMISTFT and said second PMISTFT is substituted by one of a diode and a series combination of a diode and a resistor.

31. A display device according to claim 19, wherein said display device is a liquid crystal display device.

32. A display device according to claim 20, wherein said display device is a liquid crystal display device.

33. A display device according to claim 21, wherein said display device is a liquid crystal display device.

34. A display device according to claim 22, wherein said display device is a liquid crystal display device.

35. A display device according to claim 23, wherein said display device is a liquid crystal display device.

36. A display device according to claim 24, wherein said display device is a liquid crystal display device.

37. A display device according to claim 25, wherein said display device is a liquid crystal display device.

38. A display device according to claim 26, wherein said display device is a liquid crystal display device.

39. A display device according to claim 27, wherein said display device is a liquid crystal display device.

40. A display device according to claim 28, wherein said display device is a liquid crystal display device.

41. A display device according to claim 29, wherein said display device is a liquid crystal display device.

42. A display device according to claim 30, wherein said display device is a liquid crystal display device.